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PATENT

Docket No.: Bays 10-8-2
[D8143-00206]

REMARKS

Specification

The Examiner has objected to the Title as not being descriptive of the invention. Applicant hereby amends the Title to "PROCESSOR SYSTEM INCLUDING INTERNAL ADDRESS GENERATOR FOR IMPLEMENTING SINGLE AND BURST DATA TRANSFERS". Accordingly, reconsideration and withdrawal of this objection is requested.

Drawings

The Examiner objects to Figure under 37 C.F.R. 1.83(a) as failing to show a "RDN" signal line referenced at page 5, lines 18-19 of the specification. Applicant submits herewith a revised version of Figure 1 (with changes in red) which shows the RDN signal line emanating from the internal address generator 122. Consideration and approval of this drawing change is hereby requested.

The Examiner also objects to Figure 1 because the chip select (CS) line 133 coupling the internal address generator 122 to the memory 125 is a 32-bit line, rather than a 5-bit line. However, a 32-bit line is what is required for proper operation of the device. As is well known in the art, the CS line provides a strobe signal to select a particular location. In this case, the strobe signal selects one (1) of thirty-two (32) possible memory locations. A 5-bit CS line will not accomplish this objective. Thus, no change to Figure 1 is required.

Objections

Claim 7 is objected to as containing informalities. Claim 7 has been amended as suggested by the Examiner (to change "cycles" to "cycle"), and therefore reconsideration and withdrawal of this objection is respectfully requested.

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§103 Rejections

Claims 1-8 and 10-15 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Evoy et al. (U.S. Pat. No. 6,085,307) in view of McCarthy (U.S. Pat. No. 6,321,310). For the reasons outlined below, this ground of rejection is respectfully traversed.

The present application discloses a dual processor system 100 which includes a main processor 110 and a co-processor 120. The co-processor 120 includes a control register 121, an internal address generator 122, a data register 123 and memory 125. The internal address generator 122 utilizes a control word supplied by the main processor 110 on data bus 144 to 'generate' memory locations within the memory 125 in which incoming data will be stored.

The generation of memory locations by the internal address generator 122 permits multiple data words to be stored in memory 125 quickly and efficiently, as it eliminates the need for the main processor 110 to specify the memory location of each data word (See page 1, lines 22-26 and page 5, 27-31).

Evoy teaches a master-slave processor system 10 which includes a master processor 40 and a slave processor 50. The master processor 40 controls the operational state of the slave processor by programming internal control registers 56 of the slave processor 50. The system 10 also includes a system memory 25, which, as correctly pointed out by the Examiner, is shared by both the master and slave processors 40, 50.

Evoy fails to disclose or suggest an "internal memory" (internal to the "second processor"), a "data register" or a "internal address generator" as specified in claim 1. Furthermore, Evoy fails to disclose or suggest any component which 'generates' or 'selects' memory locations for storage of incoming data.

At page 4 of the Office Action the Examiner states that since the slave processor 50 of Evoy includes a control register, "it would be inherent that an internal address generator would be coupled to the control register and also to [an] internal memory in order to decode the address being held in the [control register]..." The Applicant vigorously disagrees with this statement. The fact that the slave processor 50 of Evoy includes a control register does not lead to the

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conclusion that the slave processor must also include a internal address generator, in fact, such a contention is nonsensical. Furthermore, even if, arguendo, an internal address generator is inherent in each and every control register, the internal address generator 122 of the present invention does not "decode" the address being held in the control register (program counter) as contended by the Examiner. The internal address generator 122 utilizes a control word provided by the main processor 110 to generate a starting address in the memory 125 for a single data word or a stream of data words. Accordingly, for these additional reasons, reconsideration and withdrawal of this ground of rejection is respectfully requested.

The Examiner cites McCarthy for the teaching single and burst data transfers between processors. Although McCarthy may provide such a teaching, McCarthy does not disclose or suggest the elements missing from the Evoy reference, in particular, an "internal memory", a "data register" or a "internal address generator."

Claim 1 clearly recites:

> a second processor coupled to the system address bus and to the data bus...comprising a control register...an internal memory, a data register...and an internal address generator coupled to the control register and to the internal memory...the second processor enters a burst mode in which the internal address generator selects consecutive memory locations of the internal memory...[emphasis added]

Thus, claim 1 requires an "internal memory", a "data register", and an "internal address generator" which 'generates' address locations of a memory in which data is stored.

It is submitted that the Examiner has failed to establish a prima facie case of obviousness with the Evoy and McCarthy references. To establish a prima facie case of obviousness, there must be some teaching, suggestion or motivation in the prior art to make the specific change made by the applicant. In re Dance, 160 F.3d 1339, 1343 (Fed. Cir. 1998). Obviousness should be measured "at the time the invention was made" (i.e. the filing date of the application), and with no prior knowledge of the applicant's disclosure. In re Dembiczak, 175 F.3d 994, 998-999 (Fed. Cir. 1999).

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Obviousness cannot be established by hindsight combination to produce the claimed invention. In re Dance, 160 F.3d. at 1343. The Examiner must show reasons why the skilled artisan, confronted with the same problems as the inventor and with no knowledge of the claimed invention, would select the elements from the prior art references for combination in the manner claimed. In re Rouffet, 149 F.3d 1350, 1357 (Fed. Cir. 1998).

In the present case, there is no teaching or suggestion in either Evoy or McCarthy which would lead one of ordinary skill in the art to create the system recited in claim 1 of the present application. As stated above, neither Evoy nor McCarthy discloses or suggests an "internal memory", a "data register", and an "internal address generator" which 'generates' address locations of a memory in which data is stored. Accordingly, reconsideration and withdrawal of this ground of rejection with respect to claim 1, and claims 2-8 dependent thereon is respectfully requested.

Claims 9 and 16 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Evoy in view of McCarthy, and further in view of Curran et al. (U.S. Pat. No. 6,334,179). For the reasons outlined below, this ground of rejection is respectfully traversed.

As discussed above, neither Evoy not McCarthy discloses or suggests an "internal memory", a "data register", and an "internal address generator" which 'generates' address locations of a memory in which data is stored. Curran also fails to disclose or suggest such structure.

Curran teaches a digital signal processor system 1 which includes a host Random Access Memory (RAM) and shared RAM banks 6, 7. Curran does not teach or suggest an "internal memory", a "data register", and an "internal address generator" which 'generates' address locations of a memory in which data is stored as required by independent claims 1 and 10. Therefore, reconsideration and withdrawal of this ground of rejection with respect to dependent claims 9 and 16 is respectfully requested.

In view of the foregoing remarks and amendments, Applicants submit that this application is in condition for allowance at an early date, which action is earnestly solicited.

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The Assistant Commissioner for Patents is hereby authorized to charge any additional fees or credit any excess payment which may be associated with this communication to deposit account 50-1735.

Respectfully submitted,

Dated: 11-25-02

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Version With Markings to Show Changes Made

Claims

1. (Amended) A dual processor system, comprising:

(a) a first processor coupled to a system address bus and a data bus; and

(b) a second processor coupled to the system address bus and to the data bus, the second processor comprising a control register having a control register system address, an internal memory, a data register having a data register system address and coupled to the internal memory, and an internal address generator coupled to the control register and to the internal memory, wherein:

a[the] control word is written into the control register when the first processor places a control word having a burst mode bit and a starting internal address on the data bus and asserts the control register system address on the system address bus; and

the second processor enters a burst mode in which the internal address generator selects consecutive memory locations of the internal memory, starting at the starting internal address specified in the control word stored in the control register, during subsequent data transfer cycles, when the control word has a burst mode bit indicating burst mode.

2. (Unchanged) The dual processor system of claim 1, wherein the system is implemented as an integrated circuit.

3. (Unchanged) The dual processor system of claim 1 wherein the second processor remains in the burst mode only so long as the first processor asserts the data register system address on the system address bus.

4. (Unchanged) The dual processor system of claim 1, wherein, in a write burst mode, the first processor asserts the data register system address on the system address bus and writes subsequent data words on the data bus, and the internal address generator selects consecutive

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memory locations of the internal memory, starting at the starting internal address, whereby the subsequent data words are written into the consecutive memory locations.

5. (Unchanged) The dual processor system of claim 1, wherein, in a read burst mode, the first processor asserts the data register system address on the system address bus and reads subsequent data words on the data bus, the internal address generator selects consecutive memory locations of the internal memory, starting at the starting internal address, and the data register reads data words at the consecutive memory locations and places said data words on the data bus, whereby the subsequent data words are read from the consecutive memory locations by the first processor.

6. (Unchanged) The dual processor system of claim 1, wherein the second processor is a co-processor.

7. (Amended) The dual processor system of claim 1, wherein:

the control word is written into the control register when the first processor places a control word having a burst mode bit and a starting internal address on the data bus and asserts the control register system address on the system address bus; and

the second processor enters a single data transfer mode in which the internal address generator selects the starting internal address specified in the control word stored in the control register, during a next data transfer cycle[s] when the control word has a burst mode bit that does not indicate burst mode.

8. (Unchanged) The dual processor system of claim 1, wherein the first processor and second processor are intercoupled by the system address bus, the data bus, a chip select line, a read signal line, and a write signal line.

9. (Unchanged) The dual processor system of claim 1, wherein:

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the internal memory comprises a plurality of memory blocks;

the control word comprises the burst mode bit field, a memory bank field which specifies a selected memory bank of the plurality of memory banks, and an internal bank address field which specifies the starting internal bank address within the selected memory bank; and

the internal address generator determines the starting internal address from the selected memory bank and the internal bank address of the control word.

10. (Amended) An integrated circuit having a second processor for transferring data with a first processor coupled[coupleable] to the second processor via a system address bus and a data bus, the second processor comprising a control register having a control register system address, an internal memory, a data register having a data register system address and coupled to the internal memory, and an internal address generator coupled to the control register and to the internal memory, wherein:

a[the] control word is written into the control register when the first processor places a control word having a burst mode bit and a starting internal address on the data bus and asserts the control register system address on the system address bus; and

the second processor enters a burst mode in which the internal address generator selects consecutive memory locations of the internal memory, starting at the starting internal address specified in the control word stored in the control register, during subsequent data transfer cycles, when the control word has a burst mode bit indicating burst mode.

11. (Unchanged) The integrated circuit of claim 10, wherein the second processor remains in the burst mode only so long as the first processor asserts the data register system address on the system address bus.

12. (Unchanged) The integrated circuit of claim 10, wherein, in a write burst mode, the first processor asserts the data register system address on the system address bus and writes subsequent data words on the data bus, and the internal address generator selects consecutive

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memory locations of the internal memory, starting at the starting internal address, whereby the subsequent data words are written into the consecutive memory locations.

13. (Unchanged) The integrated circuit of claim 10, wherein, in a read burst mode, the first processor asserts the data register system address on the system address bus and reads subsequent data words on the data bus, the internal address generator selects consecutive memory locations of the internal memory, starting at the starting internal address, and the data register reads data words at the consecutive memory locations and places said data words on the data bus, whereby the subsequent data words are read from the consecutive memory locations by the first processor.

14. (Unchanged) The integrated circuit of claim 10, wherein the second processor is a co-processor.

15. (Unchanged) The integrated circuit of claim 10, wherein the first processor and second processor are intercoupled by the system address bus, the data bus, a chip select line, a read signal line, and a write signal line.

16. (Unchanged) The integrated circuit of claim 10, wherein:

the internal memory comprises a plurality of memory blocks;

the control word comprises the burst mode bit field, a memory bank field which specifies a selected memory bank of the plurality of memory banks, and an internal bank address field which specifies the starting internal bank address within the selected memory bank; and

the internal address generator determines the starting internal address from the selected memory bank and the internal bank address of the control word.

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